KUMARAGURU COLLEGE OF TECHNOLOGY

An autonomous Institution affiliated to Anna University, Chennai

COIMBATORE – 641049

PROPOSED CURRICULUM AND SYLLABUS

for

M.E. – VLSI DESIGN

Department of

Electronics and CommunicationEngineering

KUAMRAGURU COLLEGE OF TECHNOLGY, COIMBATORE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN

Program Educational Objectives (PEOs)

PEO 1: Graduates will excel as professionals in the fields of analog and digital VLSI design, semiconductor technology, and emerging domains of VLSI, contributing to innovation and the development of advanced electronic systems.

PEO 2: Graduates will continuously adapt to evolving technological advancements, leveraging their expertise to address challenges in academia, research, and industry while upholding ethical standards and contributing responsibly to society.

These PEOs align with the academic and professional aspirations in VLSI design while emphasizing both technical mastery and adaptability to future challenges.

Program Outcomes (POs)

PO. No	Program Outcome	Attributes
PO-01	Acquire technical competence, comprehensive knowledge and understanding the methodologies and technologies associated with land, air & naval defence systems. Apply knowledge to identify, formulate and analyse complex engineering problems.	Scholarship of Knowledge
PO-02	Having an ability to apply knowledge of science, mathematics, engineering & technology for development of defence technologies.	Critical Thinking
PO-03	Having an ability to design a component, subsystem or a system applying all the relevant standards and with realistic constraints, including operational and environmental.	Research Skill
PO-04	Acquire the skills for uses of contemporary techniques, resources and modern engineering and IT tools.	Usages of Modern Techniques
PO-05	An ability to identify, investigate, understand and analyse complex problems, apply creativity, carry out research /investigation and development work to solve practical problems related to defence technological issues.	Design, Development & Solutions
PO-06	Ability to communicate effectively in both oral and written contexts in the form of technical papers, project reports, design documents and seminar presentations. Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings	Communication, Individual &Team Work

KUAMRAGURU COLLEGE OF TECHNOLGY, COIMBATORE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN - CURRICULUM

Semester I							
Course Code	Course Name	Course Mode	No. of Hrs./week				
			Lecture	Tutorial	Practical	Project	Credit

P18VLI1201	Digital CMOS VLSI Design	Embedded – Theory & Lab	3	-	2	-	4
P18VLI1202	High Level Digital Design	Embedded – Theory & Lab	3	-	2	-	4
P18VLI1203	Verification of VLSI Circuits	Embedded – Theory & Lab	3	-	2	-	4
P18VLP1504	Scripting for VLSI	Practical	-	-	4	-	2
P18VLP1505	Professional Skill Development	Practical	-	-	2	-	1
P18VLP1706	Mini Project	Project only course	-	-	-	6	2
P18VLE____	Elective I	Theory	3	-	-	-	3
Total			**12**	**-**	**10**	**6**	**20**

Semester II							
Course Code	**Course Name**	**Course Mode**	**No. of Hrs. / week**				
			Lecture	**Tutorial**	**Practical**	**Project**	**Credit**
P18VLI2201	Analog Integrated Circuit Design	Embedded – Theory & Lab	3	-	2	-	4
P18VLI2202	VLSI Signal Processing	Embedded – Theory & Lab	3	-	2	-	4
P18VLI2203	Low Power VLSI Design	Embedded – Theory & Lab	3	-	2	-	4
P18VLT2004	Research Methodology and IPR	Theory	3	-	-	-	3
P18VLE____	Elective II	Theory	3	-	-	-	3
P18VLE____	Elective III	Theory	3	-	-	-	3
TOTAL			**18**	**-**	**6**	**-**	**21**

Semester III							
Course Code	**Course Name**	**Course Mode**	**No. of Hrs. / week**				
			Lecture	**Tutorial**	**Practical**	**Project**	**Credit**
P18VLP3701	Project Phase I	Project only course	-	-	-	24	12
TOTAL			**-**	**-**	**-**	**24**	**12**

Semester IV							
Course Code	**Course Name**	**Course Mode**	**No. of Hrs. / week**				
			Lecture	**Tutorial**	**Practical**	**Project**	**Credit**
P18VLP4701	Project Phase II	Project only course	-	-	-	30	15
TOTAL			**-**	**-**	**-**	**30**	**15**
Total Number of Credits			**68**				

List of Electives

Elective - I							
Course Code	Course Name	Course Mode	No. of Hrs./week				
			Lecture	Tutorial	Practical	Project	Credit
P18VLE1001	Data Structures	Theory	3	-	-	-	3
P18VLE1002	Machine learning for VLSI	Theory	3	-	-	-	3
P18VLE1003	Process Technology	Theory	3	-	-	-	3

Elective - II							
Course Code	Course Name	Course Mode	No. of Hrs./week				
			Lecture	Tutorial	Practical	Project	Credit
P18VLE2001	System-on-Chip	Theory	3	-	-	-	3
P18VLE2002	Nano devices and Circuit Design	Theory	3	-	-	-	3

Elective - III							
Course Code	Course Name	Course Mode	No. of Hrs./week				
			Lecture	Tutorial	Practical	Project	Credit
P18VLE2003	CAD for VLSI	Theory	3	-	-	-	3
P18VLE2004	Physical Design	Theory	3	-	-	-	3
P18VLE2005	VLSI for Wireless Communications	Theory	3	-	-	-	3
P18VLE2006	Universal Verification Methodology	Theory	3	-	-	-	3

SEMESTER I

P18VLI1201 - Digital CMOS VLSI Design	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	4	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Comprehend the static and dynamic behavior of MOSFETs by analyzing the various aspects of the MOS transistor model.	K4
CO2	Apply the knowledge of digital logic to design static CMOS combinational and sequential circuitry, including the selection of appropriate transistors and flip-flops, and translate the logic diagram into a CMOS circuit.	K3
CO3	Describe the general processing technologies of CMOS integrated circuits.	K6

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S	S	M	M			S	S
CO2	S	S	M	M			S	M
CO3	S	S	M	M			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**MOS transistor theory:** Ideal I-V Characteristics, C-V Characteristics, CMOS inverter – DC Characteristics, Noise Margin, Static load MOS inverters, NELS, NELT, HMOS, Pass transistor, Transmission gate, tristate inverter, MOSFET Models, Non-ideal I-V effects.	10
II	**CMOS circuit and layout design:** Combinational and Sequential Circuit Design, Basic physical design of simple gates, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino	8
III	**Circuit characterization:** Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation, Scaling principles	8
IV	**CMOS Subsystem Design:** Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	9
V	**CMOS Technologies:** Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Oxidation, Isolation Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, SOI. **Layout Design Rules:** Design Rule Background, Micron and Lambda Design Rules **Manufacturing Issues:** Antenna Rules, Layer Density Rules, Resolution Enhancement Rules.	10

References

1. "CMOS digital integrated circuits analysis and design", Kang Sung Mo and Leblebici Yusuf, McGraw Hill, Revised 4th Edition, January 2019.
2. "Principles of CMOS VLSI Design: A systems perspective", Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 2nd Edition, 1999.

3. "CMOS VLSI Design: A circuits & systems perspective", Neil H. E. Weste, David Harris, Addison Wesley, 4th Edition, 2010.
4. "Microchip Fabrication", Peter Van Zant, McGraw-Hill, International Edition, 5th Edition, 2005.

List of Lab Experiments

Sr. No	Name of Practical
1.	Introduction to layout design software - Microwind / VIRTUOSO
2.	To Study MOSIS (MOS Implementation System) layout Design Rules.
3.	To Study and implement n-MOS / pMOS transistor and its V-I characteristic using Microwind / VIRTUOSO
4.	To Study and implement CMOS Inverter using Microwind / VIRTUOSO
5.	To Study and implement NAND, AND gate using Microwind / VIRTUOSO
6.	To Study and implement NOR, OR gate using Microwind / VIRTUOSO
7.	To Study and implement XNOR, XOR gate using Microwind / VIRTUOSO
8.	Introduction to DSCH Software and Verilog.
9.	To Study and implement 2:1 MUX CMOS layout
10.	To Study and implement Half-Adder CMOS layout.
11.	To Study and implement CMOS Ring Oscillator CMOS layout
12.	To Study and implement Full Adder CMOS layout
13.	To Study and implement Two bit Comparator CMOS layout.
14.	To Study and implement Edge Triggered D-Flip Flop CMOS layout

P18VLI1202 - High Level Digital Design	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	4	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe digital design and apply digital logic to solve real life problems	K2
CO2	Illustrate and design the sequential logic circuits and do timing analysis	K4
CO3	Describe FPGA, FIFO, and AMBA bus designs	K6

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S	M	M	S				S
CO2	S	M	M	S			S	
CO3	S			M	S		S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	Introduction: Digital System; VLSI design Flow Combinational Design: Number System: Binary; 1's Complement; 2's Complement. Single Precision, Double precision	5
II	Arithmetic Circuits: Ripple Carry, Carry Look-Ahead, Carry Skip, Carry Increment, Tree Adder: Brent Kung, Sklansky, Kogge Stone Adder Datapath Functional Units: Comparator; Funnel Shifter, Multi Input Adder; Multiplier; Divider. Optimization: logic optimization techniques, Branch method, Petrick Methods	8
III	Sequential Design: Latch; Flip-flops; scan Flip-flop; Registers Set; Design of counters FSM: Mealy Machine; Moore Machine; Mixed Machine, FSM optimization	8
IV	Timing Analysis: Foundry Library; Liberty format; Gates: Propagation Delays; Flops: Propagation Delay; Setup time; hold Time; contamination delay; Recovery time; Removal time; Clock frequency; Jitter; Skew (source & network latency); Timing Paths; Multi-input path; Clock Budget; Multi-Clock; Multi-Cycle Path; False Path; Retiming	8
V	Introduction to FPGA: PLD; FPGA design flow, FPGA: Introduction to FPGA Boards, PLA, PLD, FPGA concepts and architecture	8
VI	Digital Design Application: FIFO Design-1; FIFO Design-2 [SNUG Papers] AMBA Bus Specification: AHB; APB;AXI;Bridge	8

References
1. https://onlinecourses.nptel.ac.in/noc21_ee39/ 2. "An Engineering Approach to Digital Design" , Fletcher, Pearson Education India, 2015. 3. "Rapid Prototyping of Digital Systems - SOPC Edition", James O Hamblen, Tyson S Hall, Michael D Furman, Springer New York, NY ,2008. 4. "Simulation and Synthesis Techniques for Asynchronous FIFO Design", Clifford E. Cummings [SNUG Paper] 5. "Simulation and Synthesis Techniques for Asynchronous FIFO Design with Asynchronous Pointer Comparisons", Clifford E Cummings, Peter Alfke [SNUG Paper] 6. ARM Specification [Latest]

List of Lab Experiments:

Sr. No	**Name of Practical**
1.	Write Verilog program for the following combinational design along with test bench to verify the design: a. 2 to 4 decoder realization using NAND gates only (structural model) b. 8 to 3 encoder with priority and without priority (behavioural model) c. 8 to 1 multiplexer using case statement and if statements d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2.	Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3.	Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1. a. Write test bench to verify the functionality of the ALU considering all possible input patterns b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state c. The acknowledge signal is set high after every operation is completed

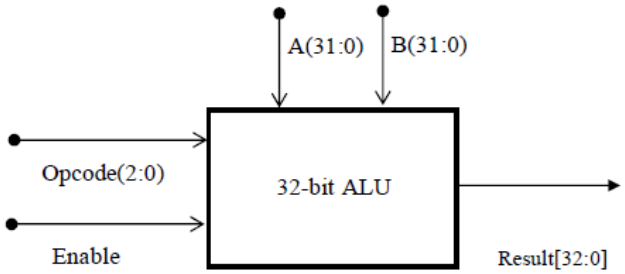

Figure 1 ALU top level block diagram

Opcode(2:0)	ALU Operation	Remarks	
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A – B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

Table 1 ALU Functions

4.	Write Verilog code for SR, D and JK and verify the flip flop.
5.	Write Verilog code for 4-bit BCD synchronous counter.
6.	Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16. Verify the functionality of the code.
7.	Write Verilog code for sequence detector 1011 using Mealy and Moore machine.
8.	Write Verilog code to design a mod-10 counter.
9.	Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rd and 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope.
10.	Interface a DC motor to FPGA and write Verilog code to change its speed and direction.
11.	Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor (i) +N steps if Switch no.1 of a Dip switch is closed (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed (iii) –N steps if Switch no. 3 of a Dip switch is closed etc.
12.	Design a FIFO using Verilog HDL
13.	Design an APB bridge using Verilog HDL

P18VLI1203 - Verification of VLSI Circuits	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	4	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe types of verification, verification plan including assertions for the digital VLSI circuits.	K2
CO2	Apply verification environments and test cases for various designs and create reusable verification IP.	K3
CO3	Explain the coverage metrics for verification process, assertions, extensible verification components, software test environments, and post silicon validation.	K6

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		M		M		S	
CO2	S		M				S	
CO3	M		M	M			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Introduction:** Verification Challenges, Productivity, Design for Verification, Methodology	3
	Types of Verifications & Approaches: Formal Verification, Property Based Verification, Functional Verification, Rule Checking-Linting, Black Box Verification, White Box Verification, Grey Box Verification	3
	Verification Planning: Planning Process, Response Checking.	3
II	**Assertions:** Specifying Assertions, Assertions on Internal DUT Signals, Assertions on External Interfaces, Assertion Coding Guidelines, Reusable Assertion-Based, Qualification of Assertions	6
	Test bench Infrastructure: Testbench Architecture, Simulation Control, Data and Transactions, Transactors, Transaction-Level Interfaces, Timing Interface, Callback Methods, Ad-Hoc Testbenches, Legacy Bus-Functional Model	6
III	**Stimulus and Response:** Generating Stimulus, Controlling Random Generation, Self-Checking Structures	4
	Coverage-Driven Verification: Coverage Metrics, Coverage Models, Functional Coverage Implementation, Feedback Mechanisms.	6
	Assertions for Formal Tools: Model Checking and Assertions, Assertions on Data	4
IV	**System-Level Verification:** Extensible Verification Components, XVC Manager, System-Level Verification Environments, Verifying Transaction-Level Models, Hardware-Assisted Verification.	4
V	**Processor Integration Verification:** Software Test Environments, Structure of Software Tests, Test Actions	3
	Post-Silicon SoC Validation: Introduction, Validation Activities, Planning for Post-Silicon Readiness, Post-Silicon Debug Infrastructure, Generation of Tests, Post-Silicon Debug	3

References

1. Verification methodology manual for SystemVerilog, Janick Bergeron, Springer, 2006th edition, 2006.
2. Writing Testbenches using System Verilog, Janick Bergeron, Springer, 1st Edition, 2006.
3. Hardware Design Verification - Simulation and Formal Method Based Approaches, William K. Lam, Pearson Prentice Hall; 1st edition, 2005.
4. A Roadmap for Formal Property Verification, Pallab Dasgupta, Springer, 2006
5. https://www.coursera.org/learn/fpga-hardware-description-languages

Lab Experiments

1. System Verilog for Adders
2. System Verilog for Flip Flops
3. System Verilog for Memory
4. System Verilog for Sequence Detectors
5. System Verilog for Interface Communication (Anyone bus protocol UART, SPI, I2C)
6. Systems Verilog for Bus Protocols (Anyone bus protocol APB, AHB, ASB)

P18VLP1504 - Scripting for VLSI	L	T	P	J	C	Total hours	
						L	P
	-	-	4	-	2	-	60

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Experiment shell scripts programmatically using different features and debugging the code.	K4
CO2	Experiment TCL scripts for VLSI for analysis of area, power and time.	K4
CO3	Experiment PERL scripts that create and change scalar, array and hash variables.	K4

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		-	S	M		S	M
CO2	S		-	S	M		S	M
CO3	S		-	S	M		S	M

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Linux:** Introduction to Linux – Linux OS structure – Types of Kernels– Linux Commands - sed – grep - awk	15
II	**TCL Scripting:** Strings – Lists – Array – Procedures - Loop Statements - Decision statements – Dictionary - File Handling - Regular Expressions & Regular Substitutions. - Namespaces - File Manipulations -Error Handling – Examples – Application of TCL in VLSI Tools	12
III	**Perl Scripting:** Introduction to PERL – Comments - Reading from Standard Input - Writing to Standard Output - Scalar Variables – Numbers and Strings - Use of Single Quotes and Double Quotes - Escape Sequence and its Usage - Use of 'chop' and 'chomp' functions Conditional Statements - Simple IF Statements - Simple IF … ELSE Statements - Multilevel IF … ELSE Statements - Looping Statements - FOR Loop - FOREACH Loop - WHILE Loop - DO … WHILE Loop - DO … UNTIL Loop - Additional Control Statements - UNLESS Statements - UNTIL Statements Loop Control Statements - LAST statement - NEXT statement - REDO statement - CONTINUE statement - Command Line Arguments **Arithmetic Operators** - Comparison Operators – Numbers and Strings - Logical Operators - Assignment Operators - Concatenation Operators - Conditional Operators - String Repetition Operators **Array Variables** – Definition - Accessing the Elements of an Array Variable - String Substitution- Ranges and Expressions - Copying Arrays - Array within Array - Size and Maximum Index of an Array - Using Array Slices - Reading an Array from Standard Input - PUSH function - POP function - SHIFT function - UNSHIFT function - REVERSE function - SORT function - Splitting and Merging the Arrays **File Handling** - Opening and Closing a File - Different types of File Modes - Reading the contents from file - Use of 'die' and 'warn' statements - Reading file to array variables - Writing the contents to the file - Standard error file - Status of a File - File Test Operators - Introduction to Hash Variables - Definition of Hash Variables - Accessing the Hash Variables - Adding the elements to the Hash Variable - Removing the elements from the Hash Variable - KEYS function - VALUES function - EACH function - EXISTS	12

	function - DELETE function **Subroutines**: Defining and Invoking a Subroutine - Forward Referencing - Passing parameters to the Subroutine - Returning a Value from Subroutine - BEGIN predefined function - END predefined function -AUTOLOAD predefined function. Use of 'strict' pragma - Defining the scope of Variables – MY, OUR and LOCAL Regular Expressions: Pattern Matching - Binding Operator (Match Operator) - Use of Metacharacters – Anchors – Alternatives - Character Range Escape Sequences - Understanding $`, $' and $& -Quantifiers-Specifying Choices - Reusing Portions of Patterns -Pattern Sequence Scalar Variables-Pattern Matching Options-Finding the Match Location - Substitution Operator - Translation Operator **Introduction to References**: Using the Backslash Operators - References to Subroutines - Special Array Indices - Use of Default Variables – '$_' and '@_' **Understanding Packages and Libraries**: "use" and "require" functions - %INC and @INC Variables - Concepts of Modularity **Process Management**: "system" function and interacting with the shell - "exec" function - %ENV hash variable- Use of back quotes **Introduction to PERL OOPS** - Working with Objects - Turning tasks into OO Programs - OOPS Terminologies - Creating own classes - 'REF' Operator - 'BLESS' Method - Storing Attributes - Creating Constructor - Considering Inheritance - Providing Attributes - Creating Methods - Distinguishing class and object methods - Get-Set Methods - Class Attributes - Privatizing the Methods - Utility Methods – Destructor - Complete Class - Adding new methods - Overriding methods - Files and Log Files - Regular Expression on various patterns. Arrays of Arrays - Arrays of Hashes - Hashes of Hashes - Hashes of Arrays	
IV	**Python Programming:** Introduction – Datatypes – Constructs – List – Tuples – Dictionary – Strings – Regular Expressions – Handling Text, CSV, XML, JSON files – Functions – Lambda functions - @ARGV array command line arguments - ARGV and the Shift functions - Array Built-in Functions - Functions: grep, split, join, slice, pop, push - Functions: shift, unshift, reverse, sort, chop, chomp - Associative Array Functions **Object oriented Python:** Classes - my function - objects, methods – destructors – Inheritance -Derives classes. **Python for VLSI:** Setting up regression - Creating Testbench Environment Structure -Developing testcases - Handling regression logs - Makefile creation - UVM RAL Model Creation Script - Regression result spreadsheet creation - Regression result HTML creation - Recursive directory manipulation	15
V	**Makefile :** Writing Makefile - Defining macros and variables	6

References

1. Programming Perl,Tom Christiansen, brian d foy, Larry Wall, Jon Orwant, 4th Edition, O'Reilly Media, Inc. February 2012,
2. Learning Linux Shell Scripting: Leverage the power of shell scripts to solve real-world problems, Ganesh Sanjiv Naik Ganesh Naik , 2nd Edition, Packtpub.
3. Mastering Linux Shell Scripting : A practical guide to Linux command-line, Bash scripting, and Shell programming, Andrew Mallett, 2nd Edition, Packtpub.
4. Beginning Linux Programming, Neil Matthew , Richard Stones, 4th edition, Wrox, 2007
5. Practical Programming in Tcl and Tk, Brent Welch, Ken Jones, Pearson; 4th edition, 2003.

Weblinks

- https://github.com/UdayaShankarS/TCL-Scripting
- https://github.com/michaelfromyeg/makefiles
- https://github.com/learnbyexample/Perl_intro

List of Experiments:

Sr. No	Name of Practical
1.	Linux Commands
2.	Shell Scripting
3.	TCL and TK scripting
4.	Makefile
5.	Perl Programming and examples
6.	Python programming and examples

P18VLP1505 - Professional Skill Development	L	T	P	J	C	Total hours	
						L	P
	-	-	2	-	1	-	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Illustrate the soft skills	K2
CO2	Illustrate the aptitude skills	K3
CO3	Illustrate the communication skills	K3

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1						M		S
CO2						M		S
CO3						M		S

Unit	Topics	No. of Hours
I	Peer interviews, mock interviews.	12
II	Logical reasoning, mathematical aptitude, domain specific problem-solving skills.	
III	Seminar	

References

1. Quantitative Aptitude for Competitive Examinations., R S Aggarwal. , S Chand, 2017.
2. Cracking the coding interview: 189 programming questions and solutions., McDowell, Gayle Laakmann. CareerCup, LLC, 2015.
3. Domain specific tools and online resources.

ELECTIVE - I

P18VLE1001 - Data Structures	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Demonstrate programs for implementation of linked lists, stack and queues.	K3
CO2	Demonstrate programs for implementation of binary search tree, sorting and searching, dictionary and Hash Table	K3
CO3	Demonstrate programs for graphs and shortest path techniques.	K3

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		-	S	M		S	M
CO2	S		-	S	M		S	M
CO3	S		-	S	M		S	M

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Algorithm specification and analysis techniques:** Analysis of recursive programs. Solving recurrence equations. General solution for a large class of recurrences.	4
II	**Elementary data structures:** Implementation of Array, lists, stacks, queues, Trees	17
III	**Sorting & Searching: B**ubble, selection, insertion, Quick sort, heap sort, merge sort. Linear search and binary search.	12
IV	**Hash Tables and Graph:** Hashing and Dictionaries. Representation of graphs. Depth First Searching. Breadth First Searching, Minimum cost spanning tree. Single source shortest paths and all-pairs shortest path	12

References

1. "Data Structures& Algorithms", Aho, Hopcroft and Ulmann, Pearson, 1st edition. 1982.
2. "Data structures and algorithm analysis in C", Mark Allen Weiss, Pearson Education India; 2nd edition, 2002.
3. "Computer Algorithms", Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran, Silicon Pr; 2nd edition,2007.
4. Introduction to Algorithms - Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. MIT Press., The MIT Press; 3rd edition, 2009

P18VLE1002 - Machine Learning for VLSI Design	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Identify the goals, applications, types and design issues of machine learning techniques.	K2
CO2	Analyse different machine learning algorithms.	K3
CO3	Describe machine learning in VLSI computer-aided design.	K3

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S	S		M	M	M		
CO2		S	S	S	s	M		
CO3		S	S	S	S	M		

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Linear and Logistic Regression** Introduction: Aims and applications of machine learning, learning systems, various aspects of developing a learning system	9

	Linear and Logistic Regression : Linear regression, Decision trees, overfitting	
II	**Instance based learning:** Instance based learning, Feature reduction, Collaborative filtering-based recommendation. **Bayesian learning:** Probability and Bayes learning	9
III	**Logistic Regression & Neural Network:** Logistic Regression, Support Vector Machine, Kernel function and Kernel SVM **Neural network:** Perceptron, multilayer network, backpropagation, introduction to deep neural network	9
IV	**Computational learning:** Computational learning theory, PAC learning model, Sample complexity, VC Dimension, Ensemble learning **Clustering**: k-means, adaptive hierarchical clustering, Gaussian mixture model	9
V	**Machine Learning in VLSI Design:** A Taxonomy for Machine Learning in VLSI Design Machine Learning for Lithographic Process Models: Masks, and Physical Design, Yield Enhancements, Machine Learning based Aging Analysis **Machine Learning Hardware:** Energy-Efficient Design of Advanced Machine Learning Hardware	9

References

1. Pattern Recognition and Machine Learning. Berlin: Springer-Verlag., Bishop, C., 2006.
2. Introduction to Machine Learning, Ethem Alpaydin, PHI,2006.
3. The Elements of Statistical Learning Data Mining, Inference, and Prediction, Trevor Hastie, Robert Tibshirani, Jerome Friedman, Second Edition, 2009.
4. Machine Learning in VLSI Computer-Aided Design., Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds, Springer, 2019.

P18VLE1003 - PROCESS TECHNOLOGY	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	Statements	K-Level
CO1	Explain the basics of semiconductor processing, lithography techniques and oxidation techniques, Si-SiO2 interface, and defects	K2
CO2	Extend the qualitative concepts of Ion Implantation, Diffusion Metallization and Outline the MOS process Integration	K2
CO3	Analyse the complete flow of thin film deposition	K4

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	M	S	S				S	
CO2	M	S	S				S	
CO3	M	S	S				S	M

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**CRYSTAL GROWTH & LITHOGRAPHY:** Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers. Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography.	12
II	**OXIDATION:** Oxidation process, techniques and systems, Modeling Oxidation, Masking Properties of Silicon Dioxide, Si-SiO2 Interface, Thin Oxides Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects.	9
III	DIFFUSION, ION IMPLANTATION & METALLIZATION Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques – Range Theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapors Deposition – Patterning	9
IV	**THIN FILM DEPOSITION** Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.	9
V	**MOS PROCESS INTEGRATION**: Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology.	6

References

1. VLSI technology, S.M. Sze, Tata McGraw-Hill, Second Edition, 2017
2. Introduction to microelectronic fabrication, R.C. Jaeger, Prentice Hall, Second Edition, 2013
3. Silicon VLSI Technology: fundamentals practice and Modeling, James D Plummer, Michael D. Deal, Peter B.Griffin, Prentice Hall India, 2009.

SEMESTER II

P18VLI2201 - Analog Integrated Circuit Design	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	3	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	To learn modeling, analysis, and design of analog circuits using CMOS technologies.	K4
CO2	Identify the principles of analog circuits and apply the techniques for the design of CMOS analog integrated circuits.	K1
CO3	Apply the methods learned in the class to design and implement practical projects	K3

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		M		M		S	
CO2	S		M				S	
CO3	M		M	M			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**CMOS Amplifiers:** Amplification – need for amplification, basic concepts, Important performance parameters – Analog Design Octagon, Common Source (CS) Amplifier-Derivation for Av and comparison of CS Amplifier with: Passive resistor load, MOSFET/Diode-Connected/Active load, Current source load - Common Drain Amplifier (or Source Follower)-Derivation for Av and comparison of CD Amplifier with: Passive resistor load, MOSFET/Diode-Connected /Active load, Current source load - Common Gate Amplifier-Derivation for Av and comparison of CG Amplifier with: Passive resistor load, MOSFET/Diode-Connected/Active load, Current source load - The Push-Pull Amplifier, Noise and Distortion in Amplifiers-A class AB Amplifier - Modeling Amplifier Noise The Source Coupled Pair- Current Source Load, Common-Mode Rejection Ratio, Noise, Matching Considerations. The Source Cross-Coupled Pair-Current Source Load Cascode Loads, Wide-Swing Differential Amplifiers, Current Differential Amplifier, Constant Transconductance Diff-Amp.	09
II	**Frequency Response & Noise characteristics of Amplifiers** Introduction, Frequency response of single stage amplifiers, Frequency response of Differential pair. Statistical characteristics of noise, types of noise, representation of noise in circuits, noise in single-stage amplifiers, noise in differential pairs, noise bandwidth. **Operational Amplifiers** Basic CMOS Op-Amp Design-Characterizing the op-Amp, Compensating the Op-amp Without Buffer, The Cascode Input Op-amp, Operational Transconductance Amplifiers.	09
III	**Nonlinear & Dynamic Analog Circuits** Design of Basic CMOS Comparator, Characterizing the Comparator Adaptive Biasing, Analog Multipliers- The Multiplying Quad, Level Shifting, Multiplier Design Using Squaring Circuits.	09

	Data Converter Fundamentals and Architectures: The MOSFET Switch - Switched-Capacitor Integrator Circuits - Sample-and-Hold (S\H) Characteristics, DAC and ADC Specifications, Architectures – Cyclic DAC, Pipeline DAC, Pipeline ADC, Integrating ADCs, SAR ADC	
IV	**Analog MOSFET Models, Current Source & Sinks** Low frequency MOSFET Model: Small-signal model of the MOSFET in saturation, Derivation for g_m and r_0 High frequency MOSFET Model: Variation of transconductance with frequency Current Source, current Sink and Current Mirror – Differences, Applications, Current Mirror-Basic current mirror, The cascode current mirror – advantages, derivation, for o/p resistance r0, Layout of current Sources/Sinks/Mirrors, Matching in MOSFET mirrors, Other Current Sources /Sinks/Mirrors- Wilson current mirror, Regulated cascode current mirror	09
V	**Voltage References** Voltage Dividers, Sensitivity and Fractional temperature coefficients-Resistor-MOSFET divider, MOSFET-only voltage divider, Current Source Self-Biasing-Threshold voltage referenced self-biasing, Diode referenced self-biasing, Thermal voltage referenced self-biasing, Bandgap voltage references, Bandgap referenced biasing, Beta Multiplier Referenced Self-Biasing-A voltage reference, Operation in the Sub-threshold region	09

References

1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998.
2. "Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000.
3. "Analog Integrated Circuit Design ", Johns & Martin, John Wiley & Sons, 1997.
4. "CMOS Analog Design", 2nd Ed, Allen & Holberg, Oxford Univ. Press, 1987.
5. "Analysis and Design of Analog Integrated Circuits" Gray & Meyer, John Wiley & Sons, 1984.
6. "Analog VLSI", Mohammed Ismail and Terri Fiez, McGraw-Hill, Inc.
7. "VLSI - Design Techniques for Analog and Digital Circuits", Geiger, Allen, & Strader McGraw-Hill, Inc.,
8. Recent papers from IEEE Journal of Solid state Circuits and other technical magazines

List of Experiments:

Sr. No	Name of Practical
1.	Characterization of NMOS and PMOS Transistor
2.	Design of Common Source Amplifier with different loads
3.	Design of Common Gate Amplifier
4.	Design of Common Drain Amplifiers
5.	Design of Single Stage Cascode Amplifiers
6.	Design of Current Mirrors
7.	Design of Differential Amplifiers with Different Loads
8.	Design of Two Stage Opamp
9.	Design of Telescopic Cascode Opamp
10.	Design of Folded Cascode Opamp
11.	Design of 6T-SRAM
12.	Transient analysis of RC Delay model
13.	Analysis of frequency response of Current series and current shunt feedback topologies
14	Analysis of frequency response of voltage series and voltage shunt feedback topologies.
15	Analysis of Circuits - Power Planning, Layout Generation, LVS, and Back annotation, total power estimation

P18VLI2202 - VLSI Signal Processing	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	4	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Analyze concepts of signal processing techniques in VLSI perspective	K3
CO2	Perform algorithmic transformations utilizing the methods of pipelining, retiming, and unfolding.	K3
CO3	Perform Algorithmic strength reduction to develop high speed and low power systems.	K3

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S	S		M	M	M	S	S
CO2		S	S	S	s	M		S
CO3		S	S	S	S	M		S

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Introduction and Iteration bound.** Introduction to DSP systems - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations. **Iteration Bound:** Introduction - Loop Bound and Iteration Bound - Algorithms for **Computing Iteration Bound:** Longest Path Matrix and Multiple Cycle Mean algorithms, Iteration Bound of Multi-rate Data Flow Graphs.	9
II	**Pipelining and Parallel Processing, Retiming** Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. **Retiming:** Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.	9
III	**Unfolding and Folding** Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	9
IV	**Systolic Architecture Design and Fast Convolution** Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays. Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution	9
V	**Bit Level Arithmetic Architectures** Introduction-Parallel Multipliers, Bit Serial Multipliers, Bit serial filter design and implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic.	9

References
1. Keshab K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, Reprint, Wiley, Inter Science, 2014.
2. Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, 2014.
3. Digital Signal Processing for Multimedia Systems", Keshab K. Parhi and Takao Nishitani, Marcel Dekker, Inc., 2004
4. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, PHI, 2010.
5. Proakis, J.G., Digital Filters: Analysis, Design and Application, McGraw Hill (1981) 2nd ed.

LAB COMPONENT

LIST OF EXPERIMENTS

1. Implementation of FIR & IIR filters
2. Implementation of FIR using pipelining and parallel processing
3. Implementation of DSP algorithms using systolic Architectures
   - FIR Filter
   - Matrix Multiplication
4. Implementation of FFT Algorithm
5. Implementation of bit serial multiplier

P18VLI2203 - Low Power VLSI Design	L	T	P	J	C	Total hours	
						L	P
	3	-	2	-	4	45	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe various components of power in CMOS VLSI Design.	K1
CO2	Comprehend various leakage power reduction techniques, technology and scaling related aspects of low power VLSI design.	K2
CO3	Explain dynamic power reduction techniques and system level issues	K6

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		M		M		S	S
CO2	S		M				S	S
CO3	M		M	M			S	M

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Introduction to Low Power Design**	2
	Overview of power dissipation in CMOS: Dynamic and Static power components, Leakage current components, Factors affecting leakage power, Examples	6
II	**Circuit techniques for leakage power reduction:** Stacking – natural and artificial, Multiple V_{th} techniques - Multiple Channel Doping's, Multiple Oxide CMOS (MOXCMOS) Circuits, Multiple Channel Lengths, Multiple Body Biases, Multi-threshold-voltage CMOS (MTCMOS), Dual Threshold CMOS, Variable Threshold CMOS (VTMOS), Dynamic Threshold CMOS (DTMOS), Dynamic V_{th} techniques – V_{th} hopping scheme, Dynamic voltage scaling (DVTS) scheme.	8
III	**Technology scaling for dynamic power reduction:** Scaling techniques – constant voltage, constant field and lateral scaling. **Voltage scaling approaches:** Reliability-Driven Voltage Scaling, Technology-Driven Voltage Scaling, Energy x Delay Minimum Based Voltage Scaling, Voltage Scaling through Optimal Transistor Sizing, Voltage Scaling using Threshold Reduction, Architecture-Driven Voltage Scaling.	8
IV	**Glitch power**: Generated and propagated glitches, Glitch power analysis, Reduction techniques, Gate triggering approach.	4
	Clock gating: Principle, Combinational and sequential clock gating, Clock gating efficiency.	4
	Adiabatic techniques for low power	2
V	Logic optimization for low power, Power modelling, Power analysis	4
	System level issues in multi-voltage designs, Level shifters	4
	Low power design of building blocks	3

References

1. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy and Sharat C. Prasad, Wiley-Interscience, 2000.
2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.

3. “Low Power Design Methodologies”, J. Rabaey & M. Pedram, Kluwer Academic Pubs. 1996.
4. “Low – Power Digital VLSI Design, Circuits and Systems”, Bellaour & M.I. Elamstry, Kluwer Academic Publishers, 1996.
5. “Logic synthesis for Low – power VLSI Designs”, S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.
6. “Practical Low Power Digital VLSI Design”, B.G.K.Yeap, Kluwer Academic Publishers, 1998.
7. “Power Aware Design Methodologies”, Pedram, Massoud, Rabaey, Jan M., Kluwer Academic Publishers.
8. “Low-power Digital Systems Based on Adiabatic- Switching Principles”, W.C. Athas, L. Swensson, J.G. Koller and E. Chou, IEEE Transactions on VLSI Systems, vol. 2, pp. 398-407, December 1994.
9. “A survey of power estimation techniques in VLSI circuits”, F. Najm, IEEE Transactions on VLSI Systems, vol. 2, pp. 446-455, December 1994.

P18VLT2004 - RESEARCH METHODOLOGY AND IPR	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	1	-	30

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Interpret the research problem, ethics and research process	K3
CO2	Illustrate the adequate knowledge on patent and rights	K4
CO3	Explore on various IPR components and process of filing.	K3

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	M	S	S	M		S		S
CO2	M	S	S	M		S		S
CO3	M	S	S	M		S		S

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**RESEARCH PROBLEM AND SCOPE FOR SOLUTION** Meaning of research problem – Sources of research problem – Criteria Characteristics of a good research problem – Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem - data collection - analysis – interpretation – Necessary instrumentations.	9
II	**FORMAT :** Effective literature studies approaches – analysis – Plagiarism – Research ethics - Effective technical writing – how to write report – Paper Developing a Research Proposal – Format of research proposal – A presentation and assessment by a review committee.	9
III	**PROCESS AND DEVELOPMENT :** Nature of Intellectual Property: Patents – Designs – Trade and Copyright - Process of Patenting and Development – Technological research – Innovation – Patenting – Development. International Scenario: International cooperation on Intellectual Property – Procedure for grants of patents – Patenting under PCT	9
IV	**PATENT RIGHTS:** Patent Rights: Scope of Patent Rights – Licensing and transfer of technology – Patent information and databases – Patenting under PCT	9
V	**NEW DEVELOPMENT IN IPR** New Development in IPR: Administration of Patent System – New developments in IPR – IPR of Biological Systems – Computer Software etc – Traditional knowledge Case Studies – IPR and IITs	9

References

1. Research methodology: and introduction for science & engineering students, Stuart Melville and Wayne Goddard, Juta Academic; 2nd ed edition, 2014.
2. Research Methodology: A Step by Step Guide for beginners, Ranjit Kumar, SAGE Publications Pvt. Ltd; Fourth edition ,2014.
3. Resisting Intellectual Property‖, Resisting Intellectual Property, ByDebora J. Halbert, 1st Edition, 2005
4. Industrial Design for Engineers, McGraw Hill, 1992.
5. Product Design, Benjamin W. Niebel, Alan B. Draper, McGraw Hill, 1974
6. Introduction to Design‖, Morris Asimow, Prentice Hall, 1962.
7. Intellectual Property in New Technological Age‖, Robert P.Merges, Peter S.Menell, Mark A.Lemley,2016
8. Intellectual Property Rights Under WTO, T.Ramappa, S.Chand, 2008.

LAB Experiments

Labe experiments carried out using CADENCE/any equivalent tools.

1. Leakage power optimization
2. Low power input output design using clock gating technique.
3. Low Power Delay Optimized Buffer Design using CMOS Technology
4. Low power SRAM design
5. Low power Interconnect design.

ELECTIVE - II

P18VLE2001 - System-on-Chip Design	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe system architecture, identify and describe the concepts of hardware software co-design.	K_2
CO2	Interpret the various processors and memories used in the SoC Design	K_3
CO3	Describe the different hardware interconnects and hardware / software interfaces involved in SoC Design.	K_3

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	W			W			S	
CO2		M	S	S	M	M	S	
CO3		M	S	S	M	M	S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Introduction to System Approach:** System Architecture overview, Components of the System, Introducing Hardware/Software Codesign, The Driving Factors of Hardware/Software Design, The Hardware-Software Codesign space. **Electronic System Level Flow:** Specification and Modeling, Pre-Partitioning Analysis, Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	9
II	**Design Principles in SOC Architecture:** Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	3
III	**Processors:** Introduction to Processors, Processor Selection for SOC, Basic Concepts in Processor Architecture, RISC Pipeline, Basic Concepts in Processor Microarchitecture, Basic Elements in Instruction Handling, Buffers, Branches, Robust Processors	6
IV	**Memory Design:** Introduction, Overview of SOC Internal and External Memories, Scratchpads and Cache Memory, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Caches, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SOC (On-Die) Memory Systems, Board-Based (Off-Die) Memory systems, Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction.	9
V	**Hardware Interconnects:** Introduction, Overview of Interconnect Architectures, Bus Architecture, SOC Standard Buses, Analytic Bus Models, Beyond the Bus (NOC with Switch Interconnects), Some NOC Switch Examples, Layered Architecture and Network Interface Unit, Evaluating Interconnect Networks. **Hardware/Software Interfaces:** Introduction, Synchronization Schemes, Memory-Mapped Interfaces, Coprocessor Interfaces, Custom-Instruction Interfaces.	10
VI	**Application Studies:** 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	8

References

1. Michael J. Flynn, Wayne Luk, “Computer System Design System-On-Chip”, John Wiley & Sons, Inc., Publication, 2011.
2. Brain Bailey, Grant Martin, Andrew Piziali, “ESL Design and Verification: A Prescription for Electronic System-Level Methodology”, Morgan Kaufmann Publication, 2007.
3. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Codesign”, Springer, 2010.
4. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.
5. Lin, Y-L.S. (ed.), “Essential issues in SOC design: designing complex systems-on- chip”, Springer, 2006. 4. SudeepPasricha, NikilDutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morghan Kaufmann Publishers, 2008

ELECTIVE III

P18VLE2003 - CAD for VLSI	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Explain various VLSI design flows, design methods and technologies.	K2
CO2	Describe various VLSI design steps and relevant design automation tools, Explain types of synthesis,	K4
CO3	Illustrate design representations and graph based problem formulations.	K3

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S			S			S	
CO2		M	S	S			S	
CO3		M		S			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**Introduction to VLSI Design Methodologies:** The VLSI deign problem, Design domains, Design Actions, Design methods and technologies	6
II	**Review of VLSI Design Automation Tools :** Quick tour of design automation tools for various methods and levels of VLSI design, Physical Design, Verification, Design Management	8
III	**High Level Synthesis :** Introduction to Synthesis, Design representations and transformations	3
	High Level Synthesis Algorithms: Partitioning, Scheduling, Allocation algorithms	10
IV	**Floor Planning and Placement :** Floor planning concepts, Shape Functions and Floor plan sizing, Placement, Types of placement problems and algorithms	6
V	**Routing:** Local routing, Types of local routing problems, Area and Channel routing problems and algorithms, Global routing	6
VI	**Layout Compaction:** Design rules, symbolic layout, Algorithms for layout compaction.	6

References

1. "Graph theory" , Narsingh Deo (Prentice-Hall of India private ltd), Dover Publications, 2017.
2. "Graph theory" , Gibbons , Cambridge University Press.
3. "Algorithms for VLSI Design Automation" ,Sabih H. Gerez , John Wiley and Sons, 2nd Edition, 2008.
4. "High Level Synthesis -Introduction to chip and System Design" , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin, Kluwer Academic Publishers, 1992.
5. "Logic synthesis and verification algorithms" , Gary D. Hachtel, Fabio Somenzi (Kluwer Academic Publishers), Springer, 1st Edition, 2005.
6. "Computer aided logical design with emphasis on VLSI " , Frederick J Hill, Gerald R. Peterson, John Wiley & Sons Inc; 4th edition, 1993,

P18VLE2004 - Physical Design	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe CMOS logic gate design, identify physical design of simple gates, give examples logic structures.	K2
CO2	Explain procedure involved in floorplan step, placement, clock tree synthesis, routing, and extraction of layout.	K2
CO3	Classify digital testing, give examples of fault modelling and fault simulation, test single stuck at fault	K2

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		M		M		S	
CO2	S		M				S	
CO3	M		M	M			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**CMOS circuit and layout design:** CMOS logic gate design- Basic physical design of simple gates - CMOS logic structures - Clocking strategies	3
II	**Floorplan:** Technology File, Circuit Description, Design Constraints, Design Planning, Power Planning, Macro Placement, Design of Floorplan Refer VLSI Physical Design at https://archive.nptel.ac.in/courses/106/105/106105161/	4
III	**Placement:** Global Placement, Detail Placement	3
IV	**Clock tree synthesis:** Clock tree synthesis, Power Analysis	6
V	**Routing:** Global Routing, Detail Routing	6
VI	**RC extraction:** Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction	4
VII	**Back annotation:** Back annotation procedure, Back Annotation Calculation	7
VIII	**Testing:** Introduction to Digital Testing - Fault modeling - Fault Simulation - Testing for Single stuck faults - Design For Testability (DFT) - Ad-Hoc DFT - Scan based designs - Built-In Self-Test (BIST)	3

References

1. https://archive.nptel.ac.in/courses/106/105/106105161/
2. "Principles of CMOS VLSI Design: A systems perspective", Neil H. E. Weste, David Harris, Kamran Eshraghian, Third Edition, Addison Wesley,2008
3. "An introduction to VLSI physical design", Majid Sarrafzadeh, C. K. Wong, McGraw Hill, 1996.
4. "Physical design essentials: an ASIC design implementation perspective", Khosrow Golshan, Springer, 2007.
5. "Nano-CMOS circuit and physical design", Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, John Wiley and Sons, 2004.

P18VLE2005 - VLSI for Wireless Communications	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Analyse on different types of mixer circuits and to Design of power amplifier for the given specifications/ requirements	K4
CO2	Develop the components needed for phase/frequency synthesizing	K5
CO3	Analyze different phase and frequency components and different modules in transmitter architectures	K4

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S	M	W	S	S		S	
CO2	S	M	W	S	S		S	
CO3	S	M	W	S			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	COMMUNCATION CONCEPTS: CIRCUIT DESIGNER PERSPECTIVE Overview of Wireless Systems-access methods-modulation schemes- wireless channel description, path loss- multipath fading-channel model, envelope-frequency selective and fast fading.	8
II	RECEIVER ARCHITECTURES: Receiver front end- filter design, low noise amplifier- wideband LNA design, narrow band LNA-impedance matching-core amplifier.	8
III	ACTIVE AND PASSIVE MIXER: Balancing low-frequency and high-frequency case analysis- switching mixer, distortion in unbalanced switching mixer, conversion gain, noise, sampling mixer, distortion, intrinsic and extrinsic noise in single-ended sampling mixer, design methodology.	8
IV	PHASE/FREQUENCY PROCESSING COMPONENTS PLL-based frequency synthesizer- phase detector- dividers- Oscillators- Loop filter- first-order, second order- higher order filters- design approaches-implementation of a frequency synthesizer with a fractional divider.	8
V	TRANSMITTER ARCHITECTURES: Transmitter block end- design philosophy, direct conversion and other architectures- Quadrature LO generator- single ended RC- single ended LC- RC with differential stages-divider based generator, power amplifier design- specifications, power output control, PA design issues, Class A, AB/B/C/E amplifiers	6

References

1. VLSI for Wireless Communication, Bosco Leung, 2nd edition, Springer publications, Canada, 2011.
2. Fundamentals of Wireless Communication David Tse and PramodViswanath, Cambridge Press, 2005.
3. Wireless Communication, DALAL & UPENA, Oxford University Press, New Delhi, 2014.
4. High-reliability-integrated-circuits, Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, Pearson Education, 2nd Edition.

P18VLE2006 - Universal Verification Methodology	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Analyse the utility of a driver, monitor, checker, and test cases in the UVM verification environment.	K4
CO2	Explain component configuration and factory, Register Abstraction Layer and TLM communications	K2
CO3	Design test bench to verify the functionality of a design and a VIP for an IP as a project.	K5

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		M		M		S	
CO2	S		M				S	
CO3	M		M	M			S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	UVM overview: Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies. UVM Testbench and environments, Interface UVCs, System and Module UVCs, the System Verilog UVM class library	4
	Object Oriented Programming: Introduction - Object in OOP, Distributed development environment, Classes, Objects, Programs, Using generalization and inheritance, polymorphism in OOP, Downcast, Class libraries, Static methods and attributes, parameterized classes, packages and namespaces Reference: Programming in Modern C++ from https://onlinecourses.nptel.ac.in/noc22_cs103/	8
II	UVM library basics: Using UVM library, Library Base Classes, the uvm_object class, the uvm_component class, UVM configuration mechanism, TLM in UVM, UVM factory, UVM message facilities, callbacks	4
	Interface UVCs: Stimulus modeling and generation, creating the driver, creating the sequencer, connecting the driver and sequencer	8
III	Automating UVC Creation: Creating the collector and monitor, modeling topology with UVM, creating the Agent, creating the UVM verification component, creating UVM sequences, configuring the sequencer's default sequence, coordinating end-of-test, implementing protocol-specific coverage and checks, handling reset, packaging interface UVCs	5
	Component Configuration and Factory: Establish and Query Component Parent-Child Relationships, Set Up Component Virtual SystemVerilog Interfaces with uvm_config_db, Constructing Components and Transactions with UVM Factory, Implement Tests to Configure Components, Implement Tests to Override Components with Modified Behavior	4
IV	UVM Callback: Create User Callback Hooks in Component Methods, Implement Error Injection with User Defined Callbacks, Implement Component Functional Coverage with User Defined Callbacks, Review Default Callbacks in UVM Base Class.	3

	Simple Testbench integration: Testbenches and Tests, creating a simple testbench, testbench configuration, creating a test, creating meaningful tests, virtual sequencers and sequences, checking for DUT correctness, implementing a coverage model.	5
V	Stimulus generation topics: Fine control sequence generation, executing multiple sequences concurrently, using p_sequencer, using pre_body() and post_body() methods, controlling the arbitration of items, interrupt sequences, protocol layering.	3
	Register Abstraction Layer: Registers, Specification, Adapter, Integrating, Integration, Register Model Overview, Model Structure, Quirky Registers, Model Coverage, Back Door Access, Generation, Stimulus Abstraction, Memory Stimulus, Sequence Examples, Built in Sequences, Scoreboarding, Functional Coverage.	6
VI	System UVCs and Testbench Integration: Introduction, module and system UVC architecture, sub-components of module and system UVCs, module UVC configuration, the testbench, sequences, coverage, stand-In mode, scalability concerns in system verification, module UVC Directory structure.	5
	TLM Communications: TLM Push, Pull and Fifo Modes, TLM Analysis Ports, TLM Pass-Through Ports, TLM 2.0 Blocking and Non-Blocking Transport Sockets	4

References

1. https://onlinecourses.nptel.ac.in/noc22_cs103/
2. "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Sharon Rosenberg, Kathleen Meade, Lulu publishers, 2010.
3. "Getting started with UVM: A beginner's guide", Vanessa R. Cooper, Verilab publisher, 2013.
4. UVM Cookbook, Verification Academy, 2013.
5. UVM User's guide, Accellera, 2011.

P18VLE2002 - NANO DEVICES AND CIRCUIT DESIGN	L	T	P	J	C	Total hours	
						L	P
	3	-	-	-	3	45	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Describe system architecture, identify hardware software co-design, give examples of co-design space, explain specification & modelling, pre-partition, partition, analyse post-partition analysis, and describe hardware and software implementation.	K2
CO2	Review the processors and its micro-architecture and basic elements in instruction handling, recognize robust processors.	K2
CO3	Describe on and off-die memories, explain memories in system on chip, compare memory systems, cache memory, model memories, interconnects in system on chip, explain network on chip.	K6

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1	S		S				S	
CO2	S		S				S	
CO3	S		S				S	

Direct	Indirect
1. Internal Test – I 2. Internal Test – II 3. Assignment 4. Group Presentation 5. End Semester Exam	Course end survey

Unit	Topics	No. of Hours
I	**MOS LIMITATIONS AND IMPROVED VERSIONS** MOSFET scaling, short channel effects, Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, volume inversion, threshold voltage, channel engineering, source/drain engineering, strain engineering, multigate technology mobility, gate stack, electron tunnelling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors	12
II	**PHYSICS OF ADVANCED MOSFET GOEMETRIES** MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect, electron tunnel current, two-dimensional confinement, scattering	9
III	**NOVEL DEVICES** Evolution of FinFET, Principle of FinFET, FinFET Schematic, Compact Drain-Current equation. Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for degenerate/non-degenerate carrier statistics CNT structure, metallic and semiconductor CNTs, energy bands in CNTs, types of CNTs: Single walled and multiwalled, physical, electrical, and thermal properties of CNTs, fabrication of CNTs. N/ P-Channel CNTFETs	9
IV	**SINGLE ELECTRONICS** Quantum dots - Coulomb blockade, Electron tunnelling devices, Single electron transistors, Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata	6
V	**CIRCUIT DESIGN USING NOVEL DEVICES** Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs	9

References

1. J P Colinge, FINFETs and other Multi-gate Transistors, Springer, Germany, 2010.
2. B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, Pan Stanford Publisher, Singapore, 2012.
3. N. Collaert, CMOS Nanoelectronics: Innovative Devices, Architectures and Applications, Reprint Pan Stanford publisher, Singapore, 2012.
4. Niraj K. Jha, Deming Chen, Nanoelectronic Circuit Design, Springer London, First Edition, 2011.
5. Rainer Waser, “Nano Electronics and Information Technology: Advanced Electronic Materials and Novel Devices”, 2nd Edition, Wiley-VCH, 2012.

Semester III

P18VLP3701 – Project Phase I	L	T	P	J	C	Total hours
	-	-	-	24	12	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Undertake innovative industry/research-oriented projects and perform feasibility analysis for finding solutions.	K5
CO2	Implement and test the proposed design using appropriate framework, programming language and tools	K5
CO3	Demonstrate an ability to present and defend project work carried out to a panel of experts	K5

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak								
	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1			S		S			S
CO2			S	M	S			S
CO3			S	M	S			S

Phase	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed requirement specification document.	
II	Design and implementation of the proposed modules with specific test cases.	
III	Detailed report of the work carried out, present, and defend the project work carried out to a panel of experts.	
References		
1. Research articles, domain specific tools and online resources.		

Semester IV

P18VLP4701 – Project Phase II	L	T	P	J	C	Total hours
				30	15	-

Course Outcome		
CO	**Statements**	**K-Level**
CO1	Undertake innovative industry/research-oriented projects and perform feasibility analysis for finding solutions.	K5
CO2	Implement and test the proposed design using appropriate framework, programming language and tools	K5
CO3	Demonstrate an ability to present and defend project work carried out to a panel of experts	K5

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

	Program Outcomes (POs)							
COs	PO1	PO2	PO3	PO4	PO5	PO6	PEO1	PEO2
CO1			S		S			S
CO2			S	M	S			S
CO3			S	M	S			S

Phase	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed requirement specification document.	
II	Design and implementation of the proposed modules with specific test cases.	
III	Detailed report of the work carried out, present, and defend the project work carried out to a panel of experts.	

References

1. Research articles, domain specific tools and online resources.