KUMARAGURU COLLEGE OF TECHNOLOGY

An autonomous Institution affiliated to Anna University, Chennai

COIMBATORE – 641049

M.E VLSI DESIGN

Curriculum and Syllabus

REGULATION 2024

Department of

Electronics and Communication Engineering

VISION

To be a centre of excellence in education and research by offering an internationally accredited curriculum, state-of-the-art infrastructure, and advanced laboratories that empower students to excel in globally competitive academic and industrial environments.

MISSION

The Department is committed to:

- Inspiring students to cultivate professional ethics, self-confidence, and leadership qualities.
- Enabling students to acquire knowledge and skills through innovative practices to address evolving global challenges and societal needs.
- Pursuing excellence in academics, core engineering domains, and research activities.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 1: Graduates will excel as professionals in the fields of analog and digital VLSI design, semiconductor technology, and emerging domains of VLSI, contributing to innovation and the development of advanced electronic systems.

PEO 2: Graduates will continuously adapt to evolving technological advancements, leveraging their expertise to address challenges in academia, research, and industry while upholding ethical standards and contributing responsibly to society.

PROGRAM OUTCOMES (POs)

Graduates of VLSI Design Postgraduate Program should have the ability to:

1. An ability to independently carry out research/investigation and development work to solve practical problems
2. An ability to write and present a substantial technical report/document
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
4. Graduates will gain expertise in designing and optimizing analog, digital, and mixed-signal VLSI systems using advanced design tools.
5. Graduates will apply emerging semiconductor technologies to develop high-performance, power-efficient VLSI solutions.
6. Graduates will embrace lifelong learning, lead responsibly, and adapt to evolving technologies through research and collaboration, ensuring readiness for academia, industry and entrepreneurship.

KUMARAGURU COLLEGE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
REGULATION 2024
M.E. VLSI DESIGN - Curriculum

Semester I

S.No.	Course code	Course Title	Course Mode	Course Type	L	T	P	J	C
1	24MAT502	Graph Theory and Optimization Techniques	Theory	BS	3	1	0	0	4
2	24VLI501	Digital CMOS VLSI Design	Embedded	PC	3	0	2	0	4
3	24VLI502	High Level Digital Design	Embedded	PC	3	0	2	0	4
4	24VLT503	Advanced Processor Architecture	Theory	PC	3	0	0	0	3
5	24VLI504	Scripting for VLSI	Embedded	PC	2	0	2	0	3
6	24INT501	Research Methodology and IPR	Theory	ES	3	0	0	0	3
								Total Credits	**21**
								Total Contact Hours/week	**24**

Semester II

S.No.	Course code	Course Title	Course Mode	Course Type	L	T	P	J	C
1	24VLI505	Analog Integrated Circuit Design	Embedded	PC	3	0	2	0	4
2	24VLI506	VLSI Signal Processing	Embedded	PC	3	0	2	0	4
3	24VLI507	Verification of VLSI Circuits	Embedded	PC	3	0	2	0	4
4	24VLT508	Low Power VLSI Design	Theory	PC	3	0	0	0	3
5	24VLE0XX	Professional Elective I	Theory	PE	3	0	0	0	3
6	24VLE0XX	Professional Elective II	Theory	PE	3	0	0	0	3
7	24VLJ509	Mini Project	Project	PW	0	0	0	6	3
								Total Credits	**24**
								Total Contact Hours/week	**30**

Semester III									
S.No.	**Course code**	**Course Title**	**Course Mode**	**Course Type**	**L**	**T**	**P**	**J**	**C**
1	24VLE0XX	Professional Elective III	Theory	PE	3	0	0	0	3
2	24VLE0XX	Professional Elective IV	Theory	PE	3	0	0	0	3
3	24VLE0XX	Professional Elective V	Theory	PE	3	0	0	0	3
4	24VLJ601	Project Phase - I	Project	PW	0	0	0	24	12
								Total Credits	**21**
								Total Contact Hours/week	**33**

Semester IV									
S.No.	**Course code**	**Course Title**	**Course Mode**	**Course Type**	**L**	**T**	**P**	**J**	**C**
1	24VLJ602	Project Phase - II	Project	PW	0	0	0	30	15
#Student can opt Project Phase - II as Internship in Industrial or Research Labs or inhouse									
								Total Credits	**15**
								Total Contact Hours/week	**30**

LIST OF ELECTIVES									
S.No.	**Course code**	**Course Title**	**Course Mode**	**Course Type**	**L**	**T**	**P**	**J**	**C**
PROFESSIONAL ELECTIVES									
1	24VLE001	Data Structures	Theory	PE	3	0	0	0	3
2	24VLE002	Nano devices and Circuit Design	Theory	PE	3	0	0	0	3
3	24VLE003	Process Technology	Theory	PE	3	0	0	0	3
4	24VLE004	Semiconductor Memories	Theory	PE	3	0	0	0	3
5	24VLE005	System-on-Chip	Theory	PE	3	0	0	0	3
6	24VLE006	VLSI Physical Design	Theory	PE	3	0	0	0	3
7	24VLE007	MEMS & NEMS	Theory	PE	3	0	0	0	3
8	24VLE008	CAD for VLSI	Theory	PE	3	0	0	0	3
9	24VLE009	Semiconductor Device Modeling	Theory	PE	3	0	0	0	3
10	24VLE010	Reconfigurable Architectures	Theory	PE	3	0	0	0	3
11	24VLE011	Modern Transistor Architectures and Circuit Performance	Theory	PE	3	0	0	0	3
12	24VLE012	VLSI for Wireless Communications	Theory	PE	3	0	0	0	3
13	24VLE013	Machine learning for VLSI	Theory	PE	3	0	0	0	3
14	24VLE014	Universal Verification Methodology	Theory	PE	3	0	0	0	3
15	24VLE015	Advanced VLSI Interconnects	Theory	PE	3	0	0	0	3

16	24VLE016	Mixed Signal Circuit Design	Theory	PE	3	0	0	0	3

Semester-wise Credits	
Semester – I	21
Semester – II	24
Semester – III	21
Semester – IV	15
Total Credits	**81**

Course types	**Credits**
Basic Science	4
Engineering Science	3
Professional Core	29
Professional Electives	15
Project/Internship	30
Total Credits	**81**

SEMESTER I

24MAT502	Graph Theory And Optimization Techniques	L	T	P	J	C
		3	1	0	0	4
BS		SDG	4,9			

Pre-requisite courses	-	Data Book / Codes / Standards (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	To introduce graph theory for solving connectivity problems
2	To teach basic graph algorithms and their applications
3	To help students model real-life problems using linear programming.
4	To provide knowledge of non-linear programming for practical problem-solving.
5	To explain the use of simulation modeling in engineering.

Course Outcomes		
After successful completion of this course, the students shall be able to		Revised Bloom's Taxonomy Levels (RBT)
CO1	To introduce graph as mathematical model to solve connectivity related problems.	U
CO2	To introduce fundamental graph algorithms.	U
CO3	To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.	Ap
CO4	To provide knowledge and training using non-linear programming under limited resources for engineering and business problems.	Ap
CO5	To understand the applications of simulation modelling in engineering problems.	U

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Designing and Optimizing analog, digital, and mixed-signal VLSI systems using advanced design tools	Apply emerging Semiconductor technologies to develop high-performance VLSI Circuits	Lifelong learning, lead responsibly, and adapt to evolving technologies for academia, industry and entrepreneurship.
1		2	2	2		2
2			2	2		2
3				2		2
4	2			2		2
5	2		2	2		2

6						2

Course Content	
GRAPHS Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.	**12 Hours**
GRAPH ALGORITHM Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms (Dijikstra's Algorithm) – Depth – First search on a graph – Theoretic algorithms (Maximum Flow Algorithms, Graph Partitioning Algorithms – Performance of graph theoretic algorithms– Graph theoretic computer languages.	**12 Hours**
LINEAR PROGRAMMING Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.	**12 Hours**
NON-LINEAR PROGRAMMING Constrained Problems – Equality constraints – Lagrangian Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming-Wolfe's method.	**12 Hours**
SIMULATION MODELLING Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.	**12 Hours**

Theory Hours:	**45**	**Tutorial Hours:**	**15**	**Practical Hours:**	**0**	**Project Hours:**	**0**	**Total Hours:**	**60**

Learning Resources

Textbooks:

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.
3. Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., “ A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012.
6. Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India,1997.

24VLI501	Digital CMOS VLSI Design	L	T	P	J	C
		3	0	2	0	4
PC		SDG	8,9,11			

Pre-requisite courses	-	Data Book / Code book (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	To understand the theory of MOS transistors, their ideal and non-ideal characteristics, and various MOS logic styles.
2	To develop knowledge in CMOS circuit design, including both combinational and sequential logic, and their physical layout techniques.
3	To introduce circuit characterization techniques like resistance, capacitance estimation, delay analysis, and power optimization.
4	To explore CMOS subsystem design elements such as data path circuits and semiconductor memory structures.
5	To study CMOS fabrication technologies, layout design rules, and manufacturing challenges to ensure reliable VLSI system design.

Course Outcomes		
After successful completion of this course, the students shall be able to		Revised Bloom's Taxonomy Levels (RBT)
CO 1	Analyze and explain the ideal and non-ideal I-V and C-V characteristics of MOSFETs and evaluate CMOS inverter DC characteristics including noise margins.	U
CO 2	Design and implement CMOS combinational and sequential logic circuits with efficient physical layout structures.	An
CO 3	Estimate and model circuit parameters such as resistance, capacitance, switching delay, and power dissipation, applying sizing and optimization techniques.	C
CO 4	Design CMOS subsystems including data path components like adders, comparators, counters, and memory units (SRAM, DRAM).	Ap
CO 5	Demonstrate understanding of CMOS fabrication processes, apply layout design rules, and address manufacturing challenges such as antenna effects and density rules.	C
CO 6	Design, simulate, and analyze CMOS layouts and digital circuits such as logic gates, multiplexers, adders, comparators, and flip-flops using layout design software like Microwind, Virtuoso, and DSCH.	C

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Designing and Optimizing analog, digital, and mixed-signal VLSI systems using	Apply emerging Semiconductor technologies to develop high-performance VLSI Circuits	Lifelong learning, lead responsibly, and adapt to evolving technologies for academia, industry
1		2	3	2	3	
2			2	2	3	
3				2	3	
4	2			2	3	
5	2		2	2	3	2
6					3	

Course Content	
MOS TRANSISTOR THEORY Ideal I-V Characteristics, C-V Characteristics, CMOS inverter – DC Characteristics, Noise Margin, Static load MOS inverters, NELS, NELT, HMOS, Pass transistor, Transmission gate, tristate inverter, MOSFET Models, Non-ideal I-V effects **Practical Component:** • To Study and implement n-MOS / pMOS transistor and its V-I characteristic • To Study and implement CMOS Inverter	**9 Hours** **6 Hours**
CMOS CIRCUIT AND LAYOUT DESIGN AND CIRCUIT CHARACTERIZATION Combinational and Sequential Circuit Design, Basic physical design of simple gates, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino logic- Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation, Scaling principles **Practical Component:** • Modify the NAND gate schematic to implement an **AND gate** using minimum additional logic. Simulate and verify the functionality. Also perform its Parasitic Extraction • Create a design for EXNOR gate and perform **Parasitic Extraction**. Simulate the extracted netlist and compare delay with the schematic simulation.	**9 Hours** **6 Hours**
INTERCONNECT AND CLOCKING STRATEGIES Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design. **Practical Component:**	**9 Hours**

• Design a SR/D/T/JK flip flops and measure its setup and hold times. • Design a UP-Down counter and measure its setup and hold times.	**6 Hours**
CMOS SUBSYSTEM DESIGN Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM. **Practical Component:** • Design and implement the full adder using CMOS logic and verify the correct operation of the Full Adder through transient simulation • Design and implement the 2 bit comparator using CMOS Logic. • Design and implement the 6T SRAM using CMOS Logic.	**9 Hours** **5 Hours**
CMOS TECHNOLOGIES Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Oxidation, Isolation Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, SOI. **Layout Design Rules:** Design Rule Background, Micron and Lambda Design Rules. **Manufacturing Issues:** Antenna Rules, Layer Density Rules, Resolution Enhancement Rules. **Practical Component:** • Generate the **layout** for the 2:1 MUX gate, perform **DRC** (Design Rule Check) and **LVS** (Layout vs Schematic) verification. • Design and implement the CMOS layout of a Ring Oscillator using Cadence Virtuoso. Perform DRC and LVS checks and verify the oscillation frequency through transient simulation.	**9 Hours** **7 Hours**

Theory Hours:	**45**	**Tutorial Hours:**	**0**	**Practical Hours:**	**30**	**Project Hours:**	**0**	**Total Hours:**	**75**

Learning Resources

Textbooks:

1. Kang Sung Mo and Leblebici Yusuf, CMOS digital integrated circuits analysis and design, McGraw Hill, Revised 4th Edition, January 2019.
2. Neil H. E. Weste, Kamran Eshraghian, Principles of CMOS VLSI Design: A systems perspective, Addison Wesley, 2nd Edition, 1999.
3. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
4. Neil H. E. Weste, David Harris, CMOS VLSI Design: A circuits & systems perspective, Addison Wesley, 4th Edition, 2010.
5. Peter Van Zant , Microchip Fabrication , McGraw-Hill, International Edition, 5th Edition, 2005.

References:

1. Seetharaman Ramachandran, ―Digital VLSI Systems design‖, 1st Edition, Springer, 2007.

2. Ming-Bo Lin, ―Introduction to VLSI Systems: A Logic, Circuit, and System Perspective‖ Indian Edition, CRC Press, 2011.
3. Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”. Second Edition, Feb 2003, Prentice Hall of India.

Online Educational Resources:

1. https://onlinecourses.nptel.ac.in/noc21_ee09/preview
2. https://onlinecourses.nptel.ac.in/noc25_ee21/preview

Assessment (Embedded course)

CAT, Activity and Learning Strategy - Think-pair-share, MCQ, End Semester Examination (ESE) Lab Workbook, Experimental Cycle tests, Viva-voce

24VLI502	High Level Digital Design	L	T	P	J	C
		3	0	2	0	4
PC		SDG	9			

Pre-requisite courses	-	Data Book / Code book (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	To introduce students to the fundamentals of high-level combinational circuit design
2	To introduce students to the fundamentals of high-level sequential circuit design
3	To develop an understanding of timing concepts in digital systems
4	To familiarize students with FPGA architectures, design flows, and simulation techniques
5	To enable students to design and implement advanced digital applications

Course Outcomes		
After successful completion of this course, the students shall be able to		**Revised Bloom's Taxonomy Levels (RBT)**
CO 1	Design and implement combinational circuits using Verilog HDL	Ap
CO 2	Analyze and optimize sequential circuits using Verilog HDL.	An
CO 3	Understand timing parameters and perform timing optimization using foundry libraries and timing paths analysis.	U
CO 4	Demonstrate simulation and synthesis of digital designs on FPGA platforms	Ap
CO 5	Design and verify advanced digital design applications.	U
CO 6	Design, simulate, and implement combinational and sequential circuits and perform timing analysis	Ap

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Designing and Optimizing analog, digital, and mixed-signal VLSI systems using	Apply emerging Semiconductor technologies to develop high-performance VLSI Circuits	Lifelong learning, lead responsibly, and adapt to evolving technologies for academia, industry and entrepreneurshi
1	2	1	2	3	3	
2	2	1	2	3	3	
3	2	1		2	2	
4	2			3	3	

5	2			2	3	
6	3		3		3	3

Course Content	
COMBINATIONAL CIRCUIT DESIGN Introduction - Digital System - VLSI design Flow - Number System: Binary 1's Complement - 2's Complement. Single Precision, Double precision. Ripple Carry- Carry Look-Ahead - Carry Skip - Carry Increment - Tree Adder - Brent Kung – Sklansky - Kogge Stone Adder. Datapath Functional Units – Comparator - Funnel Shifter - Multi Input Adder – Multiplier - Divider. **Practical Component:** • Design of Serial Adders by Verilog HDL Design of Multiplier and Divider by Verilog HDL	**9 Hours** **6 Hours**
SEQUENTIAL CIRCUIT DESIGN & OPTIMIZATION Logic optimization techniques - Branch method, Petrick Methods. Sequential Design – Latch - Flip-flops - scan Flip-flop - Registers Set - Design of counters. FSM - Mealy Machine - Moore Machine - Mixed Machine - FSM optimization **Practical Component:** • Design of Registers & Counters by Verilog HDL • Design of Sequential Machines by Verilog HDL	**9 Hours** **6 Hours**
TIMING ANALYSIS Foundry Library - Liberty format. Gates - Propagation Delays – Flops - Propagation Delay - Setup time - hold Time - contamination delay. Recovery time - Removal time - Clock frequency – Jitter - Skew (source & network latency) - Timing Paths - Multi-input path - Clock Budget - Multi- Clock - Multi-Cycle Path - False Path – Retiming. **Practical Component:** • Measure propagation delays for CMOS Inverter • Measure propagation delays for Flipflops	**9 Hours** **6 Hours**
IMPLEMENTATION STRATEGIES Introduction to FPGA – PLD - FPGA design flow - Introduction to FPGA Boards – PLA – PLD - FPGA concepts and architecture. **Practical Component:** • Simulation of digital circuits in FPGA. • Design digital systems with System Verilog.	**9 Hours** **6 Hours**
DIGITAL DESIGN APPLICATIONS Digital Design Application - FIFO Design-1 - FIFO Design-2 [SNUG Papers] AMBA Bus Specification – AHB – APB – AXI – Bridge. **Practical Component:** • Design of synchronous FIFO • Design of asynchronous FIFO	**9 Hours** **6 Hours**

Theory Hours:	45	Tutorial Hours:		Practical Hours:	30	Project Hours:		Total Hours:	75

Learning Resources
Textbooks:
1. Fletcher “An Engineering Approach to Digital Design” , , Pearson Education India, 2015. 2. James O Hamblen, Tyson S Hall, Michael D Furman, “Rapid Prototyping of Digital Systems - SOPC Edition”, Springer New York, NY ,2008.
Online Educational Resources:
https://onlinecourses.nptel.ac.in/noc21_ee39/

Assessment (Embedded course)
CAT, Activity and Learning Task(s)* , Mini project, MCQ, End Semester Examination (ESE) Lab Workbook, Experimental Cycle tests, viva-voce, etc…

24VLT503	Advanced Processor Architecture	L	T	P	J	C
		3	0	0	0	3
PC		SDG	8,9			

Pre-requisite courses	-	Data Book / Code book (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	To understand the fundamentals of CPU design, pipelining, and performance evaluation in modern computing systems.
2	To explore various parallel computer models and techniques for exploiting instruction-level parallelism (ILP).
3	To analyze the architectural features, instruction sets, and pipelining mechanisms of CISC (Pentium) and RISC (ARM) processors.
4	To evaluate memory hierarchy design, cache performance, and I/O subsystem efficiency in high-performance computing.
5	To investigate advanced processor architectures including superscalar, VLIW, SIMD, and GPGPU computing models.

Course Outcomes:		
After successful completion of this course, the students shall be able to		Revised Bloom's Taxonomy Levels (RBT)
CO1	Analyze the impact of pipelining and multicycle operations on CPU performance and identify challenges in implementation.	An
CO2	Apply instruction-level parallelism concepts using both static and dynamic techniques in modern processor architectures.	Ap
CO3	Compare and contrast the architectural design and pipelining strategies of Pentium and ARM processors.	An
CO4	Evaluate memory and I/O system performance using metrics like hit time, miss penalty, and reliability.	E
CO5	Explain and assess advanced processing architectures such as superscalar, VLIW, SIMD, and GPGPU models.	U

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Designing and Optimizing analog, digital, and mixed-signal VLSI systems using	Apply emerging Semiconductor technologies to develop high-performance VLSI Circuits	Lifelong learning, lead responsibly, and adapt to evolving technologies for academia, industry
1	2		2	3		3
2	2		2	3		3
3	2		2	3		3
4	2		2	3		3
5	2		2	3		3

Course Content	
ESSENTIALS OF COMPUTER DESIGN AND PIPELINING Fundamentals of CPU – Trends in technology, power, energy and cost, Dependability – Performance Evaluation- Instruction-Pipelining - Difficulties in Implementing Pipelines - Extending the Pipeline to Handle Multicycle Operations - Instruction Set Design and Pipelining.	**9 Hours**
THREAD LEVEL PARALLELISM & PROCESS LEVEL PARALLELISM Centralized vs. distributed shared memory-Interconnection Topologies-Multiprocessor Architecture-Symmetric Multiprocessors-Cache coherence problem-Synchronization-Memory Consistency-Multicore architecture Parallel Computer Models- Multiprocessors - ILP concepts - Compiler Techniques for Exposing ILP –Dynamic Branch Prediction – Dynamic Scheduling – Multiple instruction Issue – Hardware Based Speculation – Static scheduling -Limitations of ILP.	**9 Hours**
HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM CPU Architecture- Bus Operations – Pipelining – Branch predication – floating point unitOperating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set –addressing modes	**9 Hours**
HIGH PERFORMANCE RISC ARCHITECTURE – ARM Arcon RISC Machine – Architectural Inheritance – Core & Architectures – Registers – Pipeline– ARM Organization – ARM Processor Family – Co-Processors – ARM Instruction Set- Thumb Instruction Set – Instruction Cycle Timings – The ARM Programmer's Model – ARM Development Tools	**9 Hours**
MEMORY AND I/O Cache Performance – Reducing Cache Miss Penalty and Miss Rate – Reducing Hit Time – Main Memory and Performance – Memory Technology - Issues in	**9 Hours**

The Memory Hierarchy Design types of Storage Devices – Buses – RAID – Reliability, Availability and Dependability – I/O Performance Measures. **Advanced Processor Architectures** Introduction- Scalar Processors - Superscalar Processors - Vector Architecture – Symbolic Processors- VLIW Architectures - SIMD Extensions for Multimedia – Graphics Processing Units – Case Studies– GPGPU Computing	

Theory Hours:	**45**	**Tutorial Hours:**	**0**	**Practical Hours:**	**0**	**Project Hours:**		**Total Hours:**	**45**

Learning Resources

Textbooks:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 6th Edition, Morgan Kaufmann,2019
2. David A. Patterson, John L. Hennessy Computer Organization and Design: The Hardware/Software Interface (ARM Edition), 5th Edition (ARM-focused), Morgan Kaufmann,2016.
3. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability, Programmability, 1st Edition, McGraw-Hill, 1993
4. Andrew S. Tanenbaum, Todd Austin, Structured Computer Organization, 6th Edition, Pearson, 2012
5. William Stallings,Computer Organization and Architecture: Designing for Performance, 11th Edition, Pearson, 2019

References:

1. Joseph D. Dumas II, Computer Architecture: Fundamentals and Principles of Computer Design, CRC Press, 2017.
2. Norman P. Jouppi, Per Stenström, David A. Wood (Editors) Readings in Computer Architecture, Morgan Kaufmann, 2000.

Online Educational Resources:

https://archive.nptel.ac.in/courses/106/105/106105033/

Assessment (Theory course)

CAT, Activity and Learning Task(s), , MCQ, End Semester Examination (ESE)

24VLI504	Scripting for VLSI	L	T	P	J	C
		2	0	2	0	3
PC		SDG	4,8,9			

Pre-requisite courses	-	Data Book / Code book (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	Introduce the basics of Linux OS, commands, and text processing tools like sed, grep, and awk.
2	Develop skills in TCL scripting for file handling, regular expressions, and VLSI tool applications.
3	Build proficiency in Perl scripting, covering file operations, data structures, regular expressions, and object-oriented concepts.
4	Learn Python programming for handling data files, automation scripts, and developing VLSI verification workflows.
5	Enable writing efficient Make files to automate tasks and manage regression flows in VLSI projects.

Course Outcomes		
After successful completion of this course, the students shall be able to		Revised Bloom's Taxonomy Levels (RBT)
CO 1	Experiment with shell scripts programmatically using different features and debugging techniques.	An
CO 2	Experiment with TCL scripts for VLSI applications, focusing on the analysis of area, power, and time.	An
CO 3	Experiment with PERL scripts to create and manipulate scalar, array, and hash variables.	An
CO 4	Design and implement automation scripts using Python for VLSI tool integration and workflow management.	An
CO 5	Analyze the efficiency and performance of scripts through profiling tools and optimize them for large-scale VLSI design tasks.	An

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Designing and Optimizing analog, digital, and mixed-signal VLSI systems using advanced	Apply emerging Semiconductor technologies to develop high-performance VLSI	Lifelong learning, lead responsibly, and adapt to evolving technologies for
1	3			3	2	
2	3			3	2	
3						
4						
5	3			3	2	

Course Content	
LINUX Introduction to Linux – Linux OS structure – Types of Kernels– Linux Commands - sed – grep – awk. **Practical Component:** • Basic Linux Commands and File Management	**6 Hours** **6 Hours**
TCL SCRIPTING Strings – Lists – Array – Procedures - Loop Statements - Decision statements – Dictionary - File Handling - Regular Expressions & Regular Substitutions. - Namespaces - File Manipulations -Error Handling – Examples – Application of TCL in VLSI Tools. **Practical Component:** • Introduction to Shell Scripting and Automation	**6 Hours** **6 Hours**
PERL SCRIPTING Introduction to PERL- Conditional Statements -Additional Control Statements- Loop Control Statements- Arithmetic Operators-Array Variables-File Handling-Subroutines- Introduction to References-Understanding Packages and Libraries- Process Management-Introduction to PERL OOPS . **Practical Component:** • Exploring TCL and TK Scripting for GUI Development • Perl Scripting: Fundamentals and Practical Applications	**6 Hours** **6 Hours**
PYTHON PROGRAMMING Introduction – Datatypes – Constructs – List – Tuples – Dictionary – Strings – Regular Expressions – Handling Text, CSV, XML, JSON files – Functions – Lambda functions - @ARGV array command line arguments - ARGV and the Shift functions - Array Built-in Functions - Functions: grep, split, join, slice, pop, push - Functions: shift, unshift, reverse, sort, chop, chomp - Associative Array Functions	**6Hours**

Object oriented Python: Classes - my function - objects, methods – destructors – Inheritance -Derives classes. **Practical Component:** • Basic Python Programming: Functions and Arithmetic Operations	**6 Hours**
MAKEFILE Writing Makefile - Defining macros and variables. **Practical Component:** Makefile	**6 Hours** **6 Hours**

Theory Hours:	**30**	**Tutorial Hours:**	**0**	**Practical Hours:**	**30**	**Project Hours:**	**0**	**Total Hours:**	**60**

Learning Resources

Textbooks:

1. Programming Perl,Tom Christiansen, brian d foy, Larry Wall, Jon Orwant, 4th Edition, O'Reilly Media, Inc. February 2012,
2. Learning Linux Shell Scripting: Leverage the power of shell scripts to solve real-world problems, Ganesh Sanjiv Naik Ganesh Naik , 2nd Edition, Packtpub.

References:

1. Mastering Linux Shell Scripting : A practical guide to Linux command-line, Bash scripting, and Shell programming, Andrew Mallett, 2nd Edition, Packtpub.
2. Beginning Linux Programming, Neil Matthew , Richard Stones, 4th edition, Wrox, 2007.
3. Practical Programming in Tcl and Tk, Brent Welch, Ken Jones, Pearson; 4th edition, 2003.

Online Educational Resources:

1. https://github.com/UdayaShankarS/TCL-Scripting
2. . https://github.com/michaelfromyeg/makefiles
3. https://github.com/learnbyexample/Perl_intro

Assessment (Embedded course)

CAT, Activity and Learning Task(s)* , Mini project, MCQ, End Semester Examination (ESE) Lab Workbook, Experimental Cycle tests, viva-voce, etc…

24INT501	RESEARCH METHODOLOGY AND IPR	L	T	P	J	C
		3	0	0	0	3
ES		SDG	9,12,13			

Pre-requisite courses	-	Data Book / Code book (If any)	-

Course Objectives:	
The purpose of taking this course is to:	
1	Equip students with the knowledge and skills necessary to design, conduct and critically evaluate research
2	Draft research reports and present effective research findings
3	foster an understanding of intellectual property rights and ethical considerations essential for successful research and innovation

Course Outcomes		
After successful completion of this course, the students shall be able to		Revised Bloom's Taxonomy Levels (RBT)
CO 1	Apply the scientific method and research planning steps to formulate research problems and objectives	Ap
CO 2	Analyze different research designs and ethical considerations to classify research types and ensure ethical integrity	An
CO 3	Evaluate the structure and components of research reports to organize and present research findings effectively	E
CO 4	Interpret data collection tools and statistical methods to visualize and analyze biological research data	An
CO 5	Create a research proposal incorporating IPR principles to develop innovative and ethically sound research plans	C

Course Outcomes (CO)	Program Outcomes (PO) (Strong-3, Medium – 2, Weak-1)					
	1	2	3	4	5	6
	Independently carry out research /investigation and work	Write and present a substantial technical report/document	Demonstrate a degree of mastery over the area	Analyze and solve complex structural engineering problems	Use modern/advanced techniques, tools and skills	Communicate with larger community, to design and document complex problems
1	3	3		3	3	
2	3	3		3		
3	3			3		3
4	3	3		3		3
5	3	3		3		

Course Content	
INTRODUCTION TO RESEARCH METHODS Definition and Objectives of Research, Scientific Method, Various Steps in Scientific Research, Research Planning, Selection of a Problem for Research, Formulation of Selected Problems, Purpose of the Research, Formulation of Research Objectives, Formulation of Research Questions, Hypotheses Generation and Evaluation, Literature Search and Review Process.	**9 Hours**
RESEARCH DESIGN AND ETHICS Types and Methods of Research, Classification of Research, Research Ethics: Informed Consent, Confidentiality, Data Protection, Sampling Techniques, Methods of Collecting Primary Data, Use of Secondary Data, Experimentation, Design of Experiments, Survey Research, Construction of Questionnaires, Pilot Studies, and Pre-tests, Data Collection Methods, Processing, Editing, Classification, and Coding Validity, Reliability, Ethical Dilemmas and Solutions.	**9 Hours**
RESEARCH REPORTS Components of Research Articles, Manuscripts, Thesis, and Review Papers, Preparation of Thesis Documents: Referencing, In-text Citations, Tools like Endnote, Mendeley, Writing Techniques: CARS Model, Organizing Literature Review, Materials, and Methods Critical Thinking for Writing the Discussion Section. **Case Study:** Comparison of Research Articles with and without Referencing Tools	**9 Hours**
DATA COLLECTION AND ANALYSIS FOR RESEARCH Tools for Data Collection: Clinical Trials, Surveys, Questionnaires, Observational Methods, Data Management and Preparation, Overview of Statistical Concepts, Descriptive Statistics: Mean, Median, Mode, Variance, Standard Deviation, Data Visualization Techniques. **Case Study:** Journal Club on Research Papers Published in Tier 1 Journals	**9 Hours**
INTELLECTUAL PROPERTY RIGHTS (IPR) AND RESEARCH GRANTS Introduction to Intellectual Property Rights: Patents, Trademarks, Copyrights, Trade Secrets, Importance of IPR in Research and Innovation, developing a Research Proposal: Components, Do's and Don'ts, Writing Winning Research Proposals, Peer Review, and Feedback, Finalizing Research Plans. **Case Study:** Evaluating Successful Research Proposals and Understanding the Role of IPR	**9 Hours**

Theory Hours:	**45**	**Tutorial Hours:**	**0**	**Practical Hours:**	**0**	**Project Hours:**	**0**	**Total Hours:**	**45**

Learning Resources:
Textbooks:
1. Cooper, D. R., Schindler, P. S., & Sharma, J. K.. Business research methods (11th ed.).

Tata McGraw Hill Education. (2012)
2. Hazari, A.. Research Methodology for Allied Health Professionals. Springer Nature Singapore. (2023)
3. Goh, K. M. Research Methodology in Bioscience and Biotechnology. Springer. (2023)
4. Ganguli, P. Intellectual property rights: Unleashing the knowledge economy. McGraw Hill Education. (2017)

References:

1. AJIET. (n.d.). Lecture Notes on Research Methodology & Intellectual Property Rights. Retrieved from https://www.ajiet.edu.in/img/basic-science/21RMI56%20notes.pdf
2. Oxford University Press. (n.d.). Handbook of Intellectual Property Research: Lenses, Methods, and Perspectives. Retrieved from https://academic.oup.com/book/41122
3. Goddard, W., & Melville, S.. Research Methodology: An Introduction for Science & Engineering Students. Juta and Company Ltd. (2004)
4. Kumar, R. Research Methodology: A Step by Step Guide for Beginners (4th ed.). SAGE Publications. (2014)

Online Educational Resources:

1. https://hrdc.ugc.ac.in/Web/Home/ViewCourseDetails/842/
2. https://onlinecourses.swayam2.ac.in/ntr24_ed08/preview

Assessment (Theory course)
CAT, Activity and Learning Task(s), Mini project, MCQ, End Semester Examination (ESE)